

FIG. 1 is a plan view of a semiconductor device. The device is divided into three regions: 40: NMOS REGION, 41: PMOS REGION, and 42: NMOS REGION. The array consists of NMOS transistors (50, 51, 53, 54) and PMOS transistors (52). A dashed box labeled 60 encloses a 2x2 sub-array of transistors (51, 52, 53, 54). Labels 55, 56, 57, 58, 59, 61, 62, and 63 indicate various electrical connections and gates. Arrows L10 and L20 indicate the direction of light emission.

FIG. 10

Cross-sectional view of a memory cell array. The structure is built on a P SUBSTRATE. It features alternating N WELLS and P WELLS. NMOS transistors (labeled 62) are formed in the N WELLS, and PMOS transistors (labeled 61) are formed in the P WELLS. The gate stack consists of a conductive layer (hatched) and an insulating layer (cross-hatched). A dimension line indicates the 'MEMORY CELL ONE-BIT WIDTH' spanning one NMOS and one PMOS transistor. Reference numerals 66, 40, 71, 70, 41, 72, 69, 42, 73, and 67 point to various structural layers and regions.

FIG.13

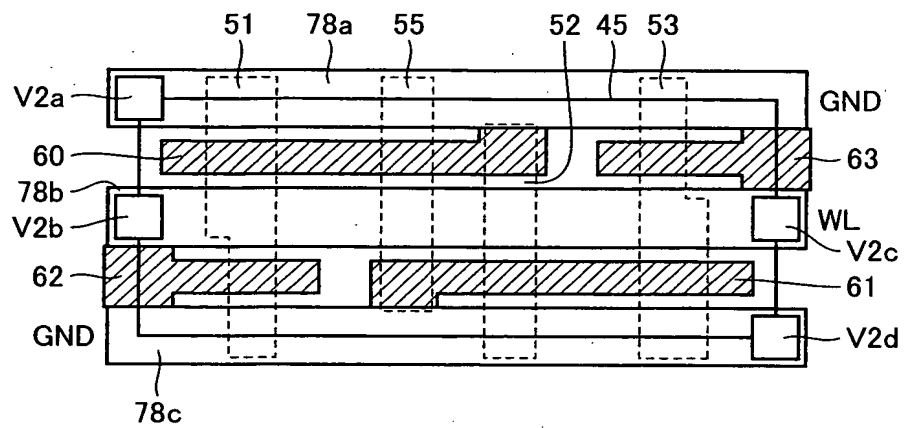


FIG.14

